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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,474	09/23/2003	Sung-Dae Cho	25611-000072/US	9061

30593 7590 04/19/2005

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EXAMINER
ANDUJAR, LEONARDO

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/667,474	CHO ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-19* is/are allowed.

6)☒ Claim(s) *1-8 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/23/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of species 3 (claims 1-20) in a communication filed on 03/09/2005 is acknowledged. Although the examiner agrees that species 1 and 2 can be considered as a single species and species 3 and 4 can be considered as another species, the restriction requirement still valid since multiple species are claimed. Furthermore, the traversal on ground(s) that the embodiments of figs. 1-7 and figs. 8-15 are sufficiently related so that their simultaneous examination would present no burden was not found persuasive. In the restriction requirement set forth in the Office Action sent on 02/09/2005, it was clearly established that the application contains claims directed to patentably distinct species wherein each species is associated to each of the different embodiments depicted in the drawings. The examination of all the species is considered a serious burden since each species contains features that make them distinct and non-obvious over the other. Therefore, a complete and independent examination would be required for each of the disclosed species. Furthermore, the criterion for restriction of species is not whether the groups are coextensive but that the claims recite mutually exclusive characteristics of such species (MPEP § 806.04(f)). To traverse on the grounds that the species are not patentably distinct, the applicant should submit evidence, or identify such evidence in the record, showing the species to be obvious variants, or clearly admit on the record that this is the case. In either case, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or

admission may be used in a rejection under 35 U.S.C. 103(a) against the other invention(s). The requirement is still deemed proper and is therefore made FINAL.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published/ under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 6, 7 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Jeung et al. (US 6,750,547).

5. Regarding claim 1, Jeung (e.g. fig. 3) shows a semiconductor package 310 comprising a substrate 120 having a top surface and a bottom surface; the top surface includes a plurality of substrate pads 123. Additionally, the package includes a semiconductor chip 130 mounted on the substrate. The semiconductor chip has an active surface, a back surface, a peripheral surface and a plurality of chip pads 133 formed on the active surface. Jeung shows a peripheral sealing portion 135 formed along the peripheral surface of the semiconductor chip and a plurality of pattern leads

140 to provide electrical connections between chip pads and substrate pads. The pattern leads extends along an inclined surface of the peripheral sealing portion

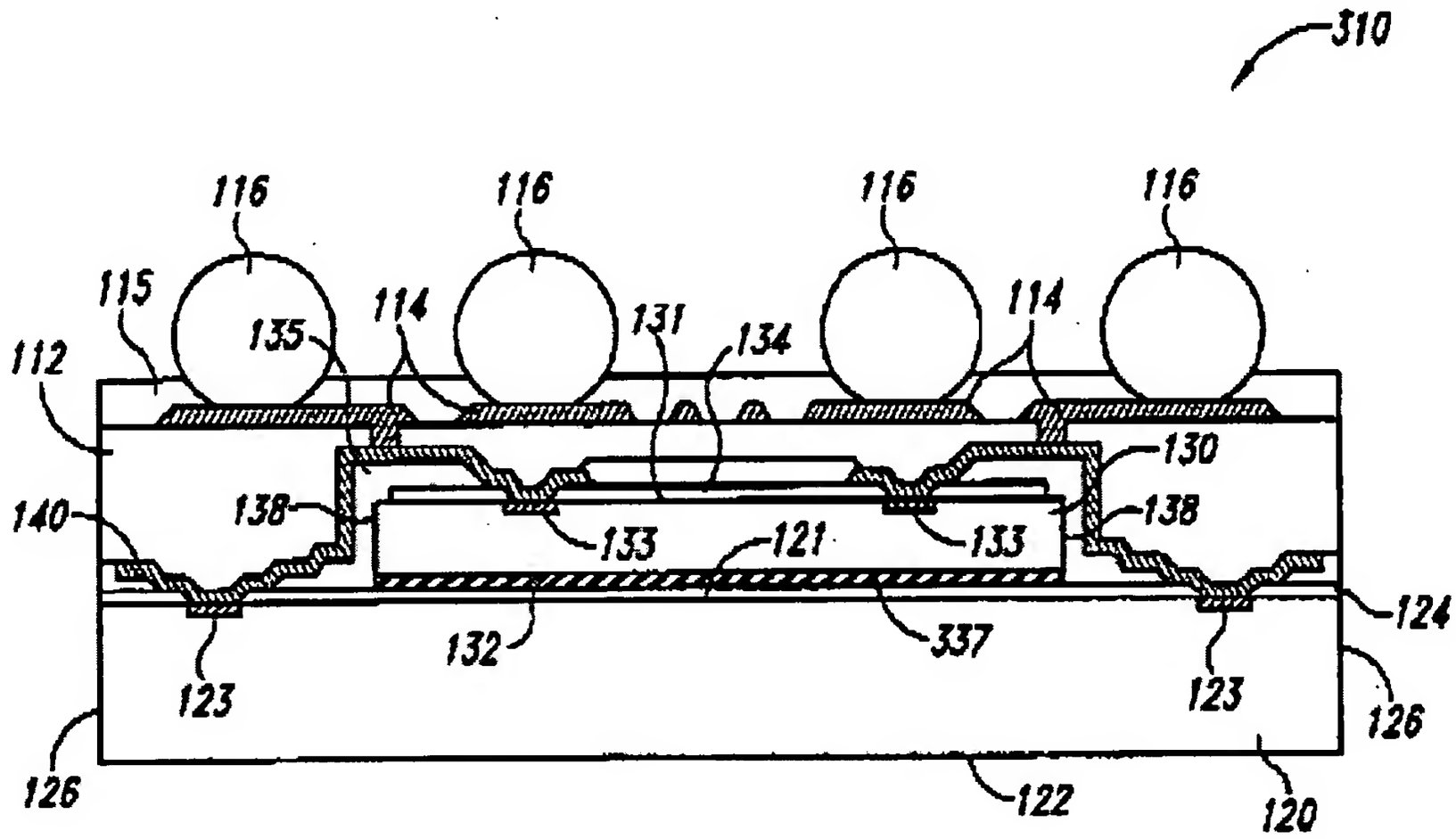


Fig. 3

6. Regarding claim 2, Jeung shows an encapsulant 112 covering the semiconductor chip, the peripheral sealing portion, the substrate pads and the pattern leads.

7. Regarding claim 3, Jeung shows that the peripheral sealing portion covers a peripheral portion of the active surface.

8. Regarding claims 4 and 6, Jeung shows external connection terminals 116 formed on the top surface of the substrate. The external connection terminals are electrically connected to the substrate pads.

9. Regarding claim 7, Jeung shows that the inclined surfaces of the peripheral sealing portion forms an angle between about 30 and 75 degrees relative to the surface of the substrate.

10. Regarding claim 20 Jeung (e.g. fig. 1A-G) shows method for manufacturing a semiconductor package comprising: mounting a semiconductor chip 130 on a substrate 120, the semiconductor chip having a plurality of chip pads 133 on an active surface and the substrate having a plurality of substrate pads 123 on a top surface; forming a first peripheral sealing portion (124, 25, 135), the first peripheral sealing portion enclosing a peripheral surface of the semiconductor chip and having an inclined surface; forming first pattern leads 140 to establish electrical connections between a first group of the chip pads and a corresponding first group of the substrate pads, the first pattern leads being formed on the inclined surface of the first peripheral sealing portion.

11. Claims 1-4, 7, 8 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Jeung et al. (US 6,747,348).

12. Regarding claim 1, Jeung (e.g. figs. 4A-4M) a semiconductor package comprising a substrate 30 having a top surface and a bottom surface, the top surface includes a plurality of substrate pads 23. Additionally, the package includes a semiconductor chip 22 mounted on the substrate. The semiconductor chip has an active surface, a back surface, a peripheral surface and a plurality of chip pads 21 formed on the active surface. Jeung shows a peripheral sealing portion 42 formed along the peripheral surface of the semiconductor chip and a plurality of pattern leads 49 to provide electrical connections between chip pads and substrate pads. The pattern leads extends along an inclined surface of the peripheral sealing portion.

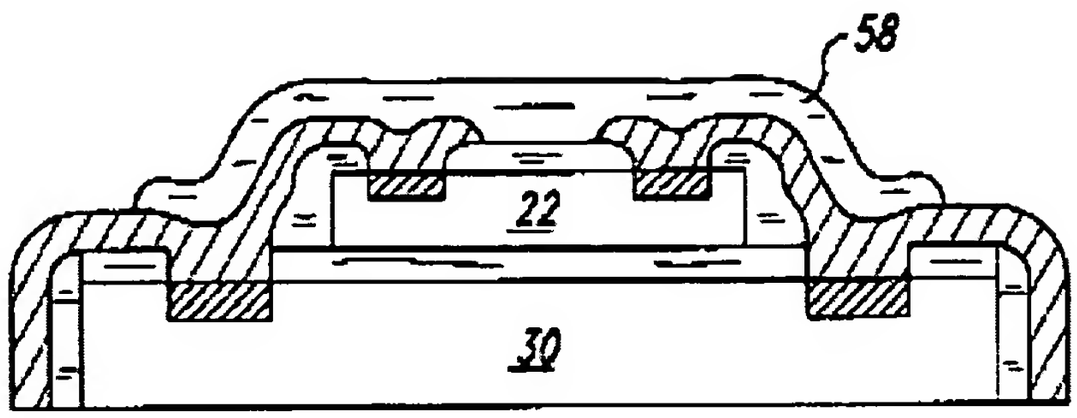


Fig. 4M

13. Regarding claim 2, Jeung shows an encapsulant 58 covering the semiconductor chip, the peripheral sealing portion, the substrate pads and the pattern leads.

14. Regarding claim 3, Jeung shows the peripheral sealing portion covers a peripheral portion of the active surface.

15. Regarding claim 4 Jeung shows external connection terminals (e.g. fig. 9) formed on the side surface substrate, the external connection terminals being electrically connected to the substrate pads.

16. Regarding claim 7, Jeung shows that the inclined surface of the peripheral sealing portion forms an angle between about 30 and 75 degrees relative to the surface of the substrate.

17. Regarding claim 8, Jeung shows that the peripheral sealing portion includes a plastic resin such as polyimide (col. 6/lls. 21-24).

18. Regarding claim 20 Jeung (e.g. fig. 4A-M) shows method for manufacturing a semiconductor package comprising: mounting a semiconductor chip 22 on a substrate 30, the semiconductor chip having a plurality of chip pads 21 on an active surface and the substrate having a plurality of substrate pads 23 on a top surface; forming a first peripheral sealing portion 42, the first peripheral sealing portion enclosing a peripheral

surface of the semiconductor chip and having an inclined surface; forming first pattern leads 49 to establish electrical connections between a first group of the chip pads and a corresponding first group of the substrate pads, the first pattern leads being formed on the inclined surface of the first peripheral sealing portion.

Claim Rejections - 35 USC § 103

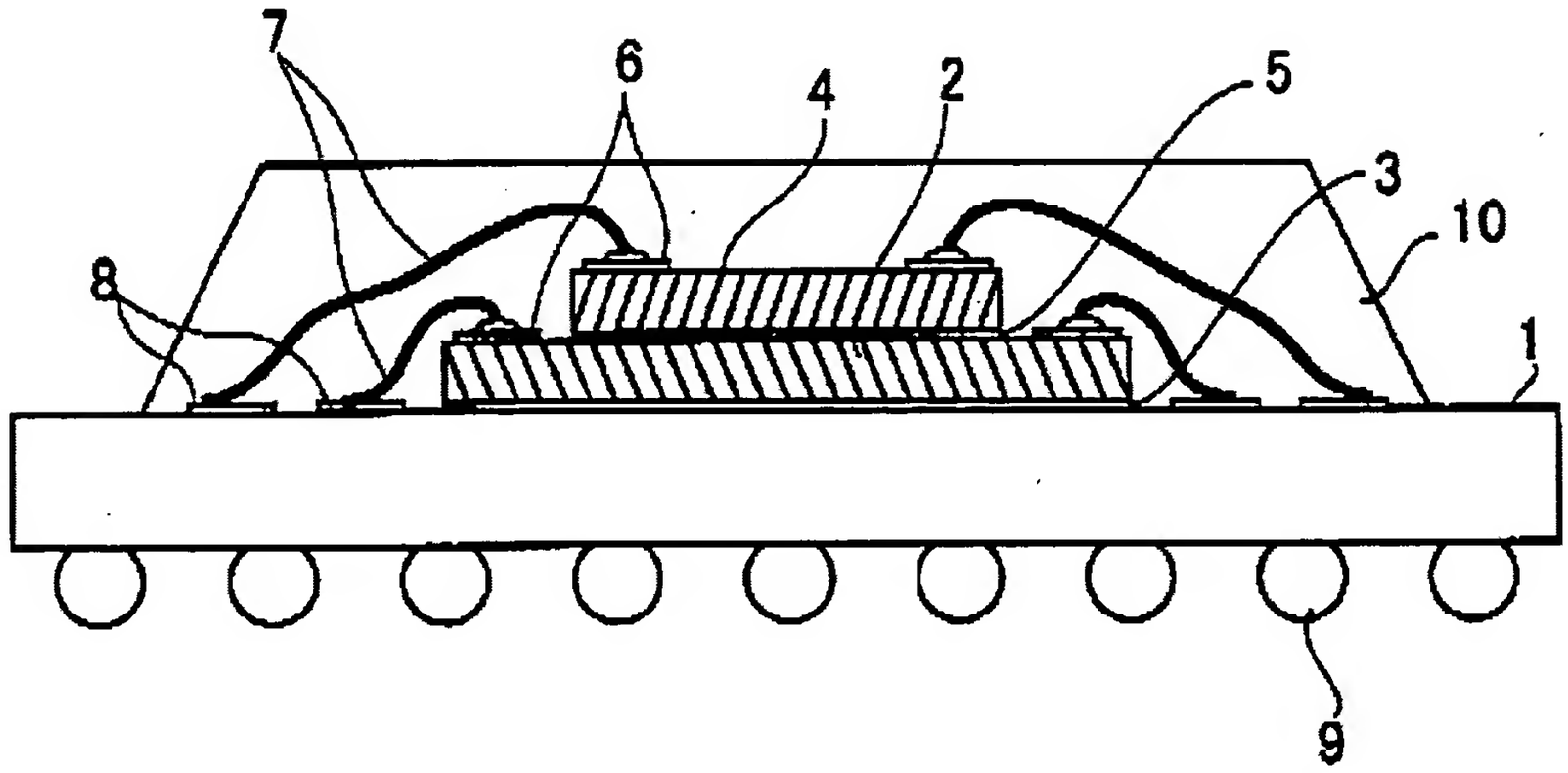
19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Uchia (US 6,437,446) in view of Jeung et al. (US 6,750,547).

21. Regarding claims 1, Uchia shows a semiconductor package comprising: a substrate 1 having a top surface and a bottom surface, the top surface including a plurality of substrate pads 8; a semiconductor chip 2 mounted on the substrate, the semiconductor chip having an active surface, a back surface, and a peripheral surface, the active surface including a plurality of chip pads 6; and a plurality of wires 7 providing electrical connections between chip pads and substrate pads. Uchia does not disclose a peripheral sealing portion formed along the peripheral surface of the semiconductor chip and a plurality of conductive leads providing electrical connections between chip pads and substrate pads and extending along an inclined surface of the peripheral sealing portion.

FIG. 1



Nevertheless, Jeung discloses a peripheral sealing portion 135 formed along the peripheral surface of the semiconductor chip and a plurality of conductive leads 140 providing electrical connections between chip pads 133 and substrate pads 123 and extending along an inclined surface of the peripheral sealing portion. This feature can have several advantages. For example, the connection structure 140 can be shorter than a corresponding wire bond coupled between the first connection sites 123 and the second connection sites 133. Accordingly, the length of time required transmitting signals between the first and second connection sites 123 and 133 can be reduced compared with devices that include wire bonds (col. 5/lls. 65-67 &col. 6/lls. 1-7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a peripheral sealing portion along the peripheral surface of the semiconductor chip disclosed by Uchia and to use a plurality of conductive leads to

provide electrical connections between chip pads and substrate pads wherein the leads are extended along an inclined surface of the peripheral sealing portion in accordance to Jeung's invention in order to reduce the time required for transmitting signals between the first and second connection sites.

22. Regarding claim 2, Jeung shows an encapsulant 112 covering the semiconductor chip, the peripheral sealing portion, the substrate pads and the pattern leads.

23. Regarding claim 3, Jeung shows the peripheral sealing portion covers a peripheral portion of the active surface.

24. Regarding claims 4, Uchia shows external connection terminals 9 formed on the bottom surface of the substrate wherein the external connection terminals are electrically connected to the substrate pads (col. 3/lls. 39-48).

25. Regarding claim 5, Uchia teaches that the external connection terminals that are arranged on the bottom surface of the substrate comprise solder balls 9 (col. 3/lls. 39-48).

26. Regarding claims 4 and 6, Jeung shows external connection terminals 116 formed on the top surface of the substrate, the external connection terminals being electrically connected to the substrate pads

27. Regarding claim 7, Jeung shows that the inclined surface of the peripheral sealing portion forms an angle between about 30 and 75 degrees relative to the surface of the substrate.

28. Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Uchia (US 6,437,446) in view of Jeung et al. (US 6,750,547) further in view of Jeung et al. (US 6,747,348).

29. Regarding claim 8, Uchia in view of Jeung ('547) teaches most aspects of the instant invention except for a peripheral portion selected from the group consisting of photo solder resist and plastic resin. Nevertheless, Jeung ('348) shows a semiconductor device having peripheral sealing portion 42 made of a plastic resin such as polyimide (col. 6/lls. 21-24). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the a peripheral portion disclosed by Uchia in view of Jeung ('547) of a plastic resin as taught by Jeung ('348), since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416*

30. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeung et al. (US 6,750,547) in view of Jeung et al. (US 6,747,348).

31. Regarding claim 8, Jeung ('547) teaches most aspects of the instant invention except for a peripheral portion selected from the group consisting of photo solder resist and plastic resin. Nevertheless, Jeung ('348) shows that a semiconductor device having peripheral sealing portion 42 made of a plastic resin such as polyimide (col. 6/lls. 21-24). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the a peripheral portion disclosed by Jeung ('547) of a plastic resin as taught by Jeung ('348), since it has been held to be within the

general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

Allowable Subject Matter

32. Claims 9-19 are allowed.

Conclusion

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonardo Andujar
Patent Examiner
04/10/2005